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A 2-GHz Low-Power Down-Conversion Mixer in 0.18- μ m CMOS Technology

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Abstract

A low-voltage and low-power RF mixer for WCDMA applications is presented. The paper presents a novel topology mixer that leads to a better performance in terms of isolation and power consumption for low supply voltage. The measuring results of the proposed mixer achieve: 7dB power conversion gain, 10.4dB double side band (DSB) noise figure, -2dBm input third-order intercept point (IIP3), and the total dc power consumption of this mixer including output buffers is 2.2mW from a 1V supply voltage. The current output buffer is about 1.96mW, the excellent LO-RF, LO-IF and RF-IF isolation achieved up to 49dB, 39.5dB and 57.3dB, respectively.

Key words : CMOS mixer; Double side band (DSB) noise figure;

Gilbert cell mixers